EAST - [kevin's workspace.wsp:1]

File View Edit Tools Window Help

- Drafts
- Pending
- Active
  - L1: (2839) (711/5,104,105,149).CCLS.
  - L2: (232843) bank
  - L3: (1084873) port
  - L4: (587137) clock
  - L5: (650991) register
  - L6: (833576) buffer
  - L7: (59230) conflict
  - L8: (108) 1 and 2 and 3 and 4 and 5 and 6 and 7
  - L9: (2642956) switch$4
  - L10: (198) 1 and 2 and 3 and 4 and 5 and 6 and 9
  - L11: (124) 10 not 8
  - L12: (42872) switch$4 adj network
  - L13: (26) 1 and 2 and 3 and 4 and 5 and 6 and 12
  - L14: (11) 13 not 8
  - L15: (2) (2 and 3 and 4 and 5 and 6 and 7 and 9).clm.
  - L16: (3) (2 and 3 and 4 and 5 and 6 and 7).clm.
  - L17: (1) (2 and 3 and 4 and 5 and 6 and 12).clm.
  - L18: (13) (2 and 3 and 4 and 5 and 6 and 9).clm.
- Failed
- Saved
- Favorites
- Tagged (4)
- UDC
- Queue
- Trash

	U		Document ID	Issue Date	Pages	Inventor	Title	Current OR	Current XR
1	☐	☐	US 20030135699 A1	20030717	200	Matsuzaki, Yasurou et al.	Multi-port memory based on DRAM core	711/149	
2	☐	☐	US 20040186945 A1	20040923	15	Jeter, Robert E. JR. et al.	System and method for dynamic mirror-bank addressing	711/5	711/162
3	☐	☐	US 6609174 B1	20030819	7	Naji; Peter K.	Embedded MRAMs including dual read ports	711/104	365/171;
4	☐	☐	US 6877071 B2	20050405	18	Sherman; David L.	Multi-ported memory	711/149	711/100;

BRS form | ISUR form | Hits | Details

Ready

NUM